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Features

- Fast Read Access Time - 90 ns
- Low Power CMOS Operation
 - 100 μ A max. Standby
 - 40 mA max. Active at 5 MHz
- JEDEC Standard Packages
 - 32 Lead PLCC
 - 32-Lead 600-mil PDIP
 - 32-Lead 450-mil SOIC (SOP)
 - 32-Lead TSOP
- 5V $\pm$ 10% Supply
- High-Reliability CMOS Technology
 - 2,000V ESD Protection
 - 200 mA Latchup Immunity
- Rapid™ Programming Algorithm - 50 μ s/byte (typical)
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Industrial and Commercial Temperature Ranges

Jameco Part Number 156275



8-Megabit (1M x 8) OTP EPROM

AT27C080

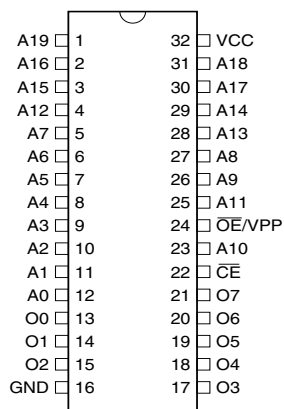
Description

The AT27C080 chip is a low-power, high-performance 8,388,608-bit one-time programmable read only memory (OTP EPROM) organized as 1M by 8 bits. The AT27C080 requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 90 ns, eliminating the need for speed reducing WAIT states on high-performance microprocessor systems. *(continued)*

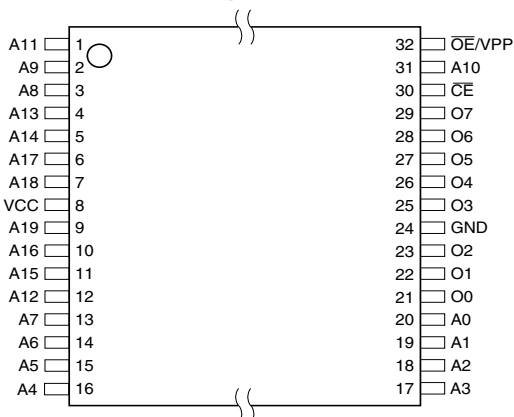
Pin Configurations

Pin Name	Function
A0 - A19	Addresses
O0 - O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}/VPP$	Output Enable/ Program Supply

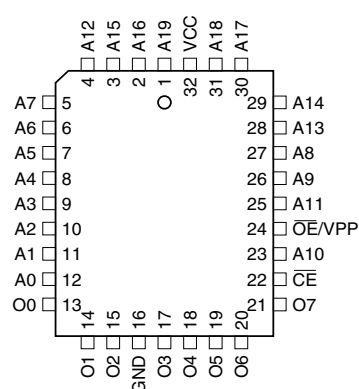
PDIP, SOIC Top View



TSOP Top View
Type 1



PLCC Top View



Rev. 0360H-03/01



Atmel's scaled CMOS technology provides low active power consumption and fast programming. Power consumption is typically 10 mA in active mode and less than 10 μ A in standby mode.

The AT27C080 is available in a choice of packages, including; one-time programmable (OTP) plastic PLCC, PDIP, SOIC (SOP), and TSOP. All devices feature two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

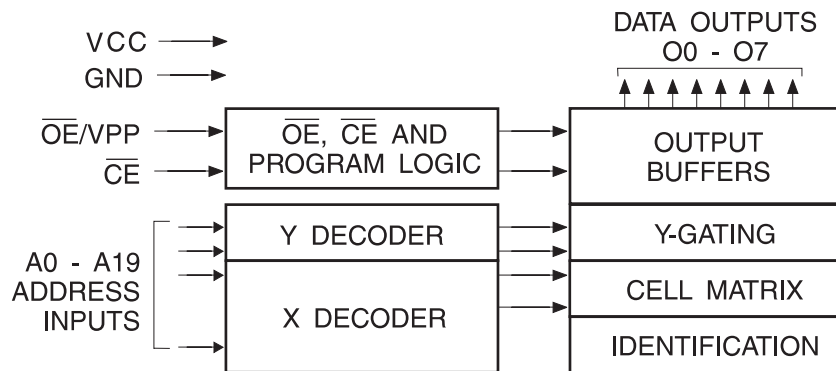
With high density 1M byte storage capability, the AT27C080 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C080 has additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 50 μ s/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 μ F high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 μ F bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V ⁽¹⁾
Voltage on A9 with Respect to Ground	-2.0V to +14.0V ⁽¹⁾
V _{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V ⁽¹⁾
Integrated UV Erase Dose	7258 W•sec/cm ²

***NOTICE:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC which may overshoot to +7.0V for pulses of less than 20 ns.

Operating Modes

Mode/Pin	$\overline{CE}$	$\overline{OE}/V_{PP}$	Ai	Outputs
Read	V _{IL}	V _{IL}	Ai	D _{OUT}
Output Disable	X	V _{IH}	X ⁽¹⁾	High Z
Standby	V _{IH}	X	X	High Z
Rapid Program ⁽²⁾	V _{IL}	V _{PP}	Ai	D _{IN}
PGM Verify	V _{IL}	V _{IL}	Ai	D _{OUT}
PGM Inhibit	V _{IH}	V _{PP}	X	High Z
Product Identification ⁽⁴⁾	V _{IL}	V _{IL}	A9 = V _H ⁽³⁾ A0 = V _{IH} or V _{IL} A1 - A19 = V _{IL}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
 2. Refer to Programming Characteristics.
 3. V_H = 12.0 ± 0.5V.
 4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

DC and AC Operating Conditions for Read Operation

		AT27C080-90	AT27C080-10	AT27C080-12	AT27C080-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V _{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
I _{LI}	Input Load Current	V _{IN} = 0V to V _{CC} (Com., Ind.)		±1.0	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0V to V _{CC} (Com., Ind.)		±5.0	μA
I _{SB}	V _{CC} ⁽¹⁾ Standby Current	I _{SB1} (CMOS), $\overline{CE} = V_{CC} \pm 0.3V$		100	μA
		I _{SB2} (TTL), $\overline{CE} = 2.0$ to V _{CC} + 0.5V		1.0	mA
I _{CC}	V _{CC} Active Current	f = 5 MHz, I _{OUT} = 0 mA, $\overline{CE} = V_{IL}$		40	mA
V _{IL}	Input Low Voltage		-0.6	0.8	V
V _{IH}	Input High Voltage		2.0	V _{CC} + 0.5	V
V _{OL}	Output Low Voltage	I _{OL} = 2.1 mA		0.4	V
V _{OH}	Output High Voltage	I _{OH} = -400 μA	2.4		V

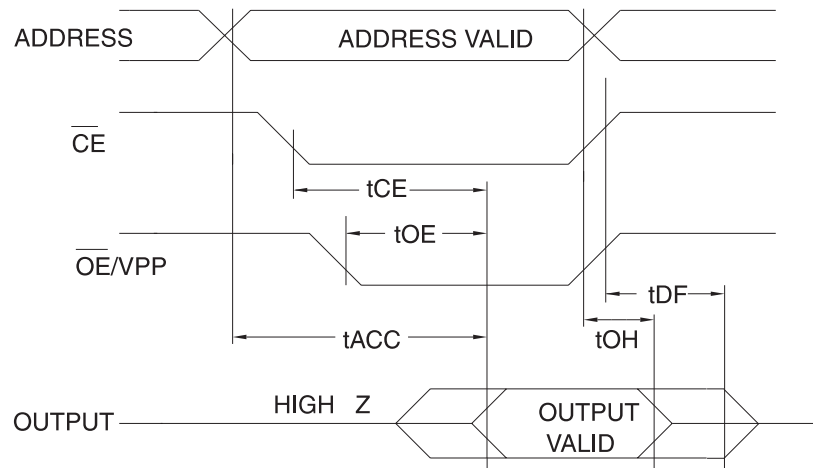
Note: 1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$, and removed simultaneously or after $\overline{OE}/V_{PP}$.

AC Characteristics for Read Operation

Symbol	Parameter	Condition	AT27C080								Units
			-90		-10		-12		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{ACC} ⁽⁴⁾	Address to Output Delay	$\overline{CE} = \overline{OE}/V_{PP}$ $= V_{IL}$		90		100		120		150	ns
t _{CE} ⁽³⁾	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		90		100		120		150	ns
t _{OE} ⁽³⁾⁽⁴⁾	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		20		20		30		35	ns
t _{DF} ⁽²⁾⁽⁵⁾	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first			30		30		35		40	ns
t _{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}/V_{PP}$ whichever occurred first		0		0		0		0		ns

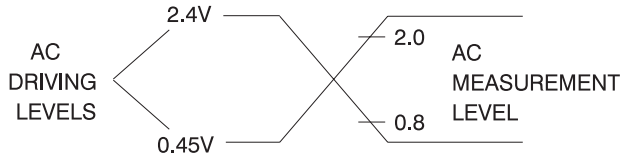
Notes: 1. 2, 3, 4, 5. See AC Waveforms for Read Operation.

AC Waveforms for Read Operation⁽¹⁾



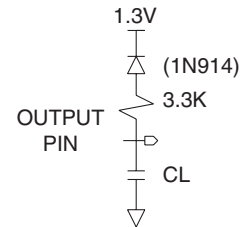
- Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
 2. t_{DF} is specified from OE/VPP or CE, whichever occurs first. Output float is defined as the point when data is no longer driven.
 3. $\overline{OE}/V_{PP}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} .
 4. $\overline{OE}/V_{PP}$ may be delayed up to $t_{ACC} - t_{OE}$ after the address is valid without impact on t_{ACC} .
 5. This parameter is only sampled and is not 100% tested.

Input Test Waveform and Measurement Levels



$t_R, t_F < 20$ ns (10% to 90%)

Output Test Load



Note: $CL = 100$ pF including jig capacitance.

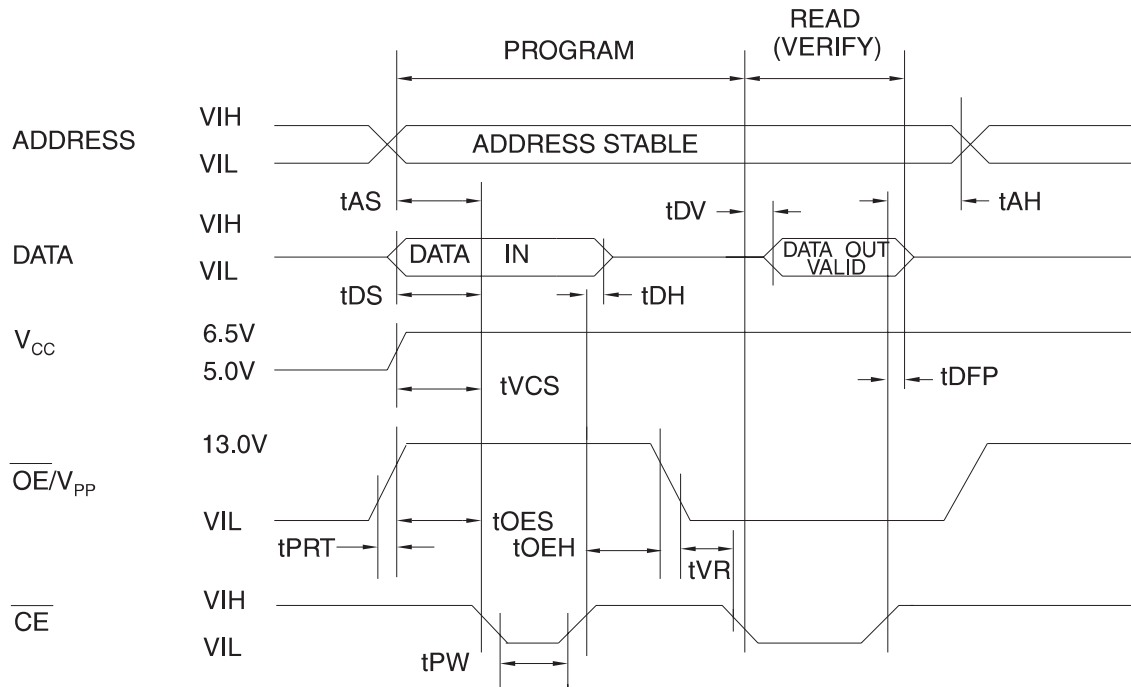
Pin Capacitance

$f = 1$ MHz, $T = 25^\circ\text{C}$ ⁽¹⁾

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	$V_{IN} = 0V$
C_{OUT}	8	12	pF	$V_{OUT} = 0V$

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms



- Notes:
1. The Input Timing reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
 2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

DC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, OE/V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I _{LI}	Input Load Current	V _{IN} = V _{IL} , V _{IH}		±10	μA
V _{IL}	Input Low Level		-0.6	0.8	V
V _{IH}	Input High Level		2.0	V _{CC} + 1.0	V
V _{OL}	Output Low Voltage	I _{OL} = 2.1 mA		0.4	V
V _{OH}	Output High Voltage	I _{OH} = -400 μA	2.4		V
I _{CC2}	V _{CC} Supply Current (Program and Verify)			40	mA
I _{PP2}	OE/V _{PP} Supply Current	CE = V _{IL}		25	mA
V _{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

$T_A = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.5 \pm 0.25\text{V}$, $\overline{\text{OE}}/V_{PP} = 13.0 \pm 0.25\text{V}$

Symbol	Parameter	Test Conditions ⁽¹⁾	Limits		Units
			Min	Max	
t_{AS}	Address Setup Time	Input Rise and Fall Times: (10% to 90%) 20 ns	2.0		μs
t_{OES}	$\overline{\text{OE}}/V_{PP}$ Setup Time		2.0		μs
t_{OEH}	$\overline{\text{OE}}/V_{PP}$ Hold Time		2.0		μs
t_{DS}	Data Setup Time		2.0		μs
t_{AH}	Address Hold Time	Input Pulse Levels: 0.45V to 2.4V	0.0		μs
t_{DH}	Data Hold Time		2.0		μs
t_{DFP}	$\overline{\text{CE}}$ High to Output Float Delay ⁽²⁾	Input Timing Reference Level: 0.8V to 2.0V	0.0	130	ns
t_{VCS}	V_{CC} Setup Time		2.0		μs
t_{PW}	$\overline{\text{CE}}$ Program Pulse Width ⁽³⁾		47.5	52.5	μs
t_{DV}	Data Valid from $\overline{\text{CE}}$	Output Timing Reference Level: 0.8V to 2.0V		1.0	μs
t_{VR}	$\overline{\text{OE}}/V_{PP}$ Recovery Time		2.0		ns
t_{PRT}	$\overline{\text{OE}}/V_{PP}$ Pulse Rise Time During Programming		50		ns

- Notes:
- V_{CC} must be applied simultaneously or before $\overline{\text{OE}}/V_{PP}$ and removed simultaneously or after $\overline{\text{OE}}/V_{PP}$
 - This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
 - Program Pulse width tolerance is $50 \mu\text{s} \pm 5\%$.

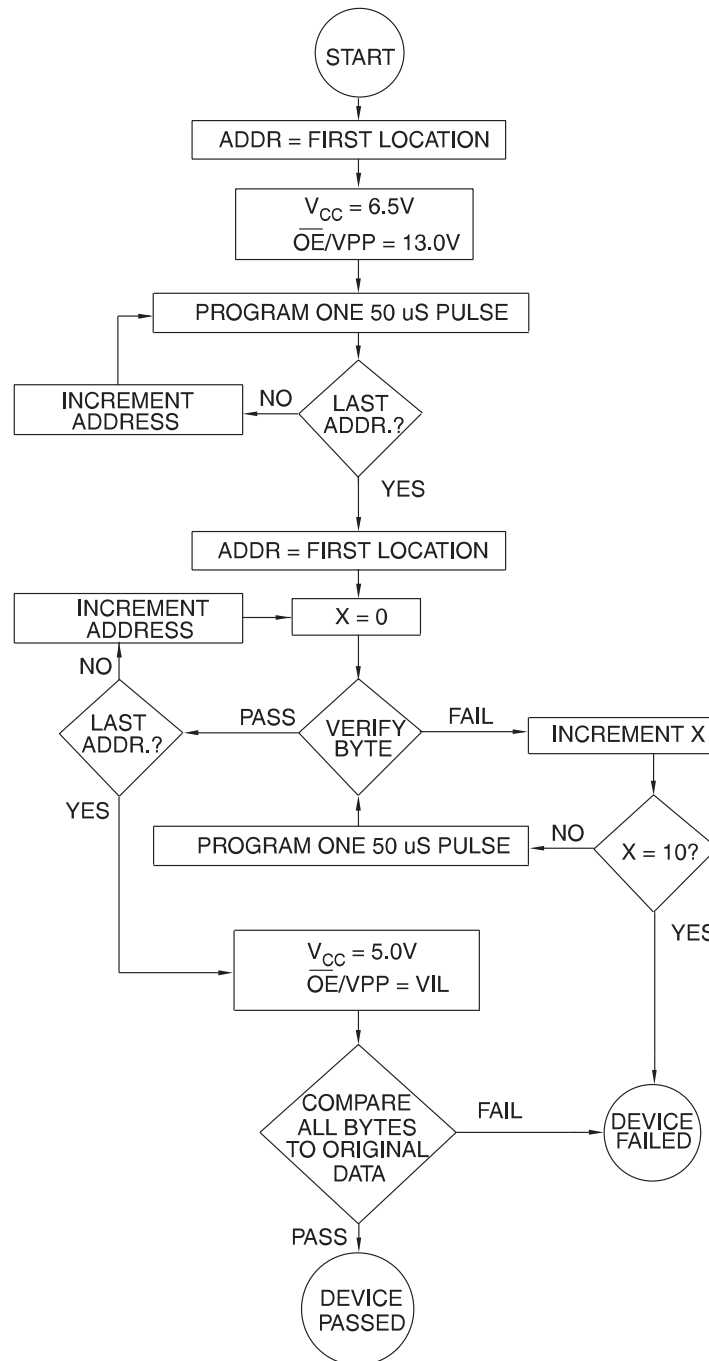
Atmel's 27C080 Integrated Product Identification Code

Codes	Pins									Hex Data
	A0	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	1	0	0	0	1	0	1	0	8A

Rapid Programming Algorithm

A 50 μs $\overline{\text{CE}}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and $\overline{\text{OE}}/V_{\text{PP}}$ is raised to 13.0V. Each address is first programmed with one 50 μs $\overline{\text{CE}}$ pulse without verification. Then a verification reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 50 μs pulses are applied with a verification after each

pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. $\overline{\text{OE}}/V_{\text{PP}}$ is then lowered to V_{IL} and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t _{ACC} (ns)	I _{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	40	0.1	AT27C080-90JC	32J	Commercial (0°C to 70°C)
			AT27C080-90PC	32P6	
			AT27C080-90RC	32R	
			AT27C080-90TC	32T	
	40	0.1	AT27C080-90JI	32J	Industrial (-40°C to 85°C)
			AT27C080-90PI	32P6	
			AT27C080-90RI	32R	
			AT27C080-90TI	32T	
100	40	0.1	AT27C080-10JC	32J	Commercial (0°C to 70°C)
			AT27C080-10PC	32P6	
			AT27C080-10RC	32R	
			AT27C080-10TC	32T	
	40	0.1	AT27C080-10JI	32J	Industrial (-40°C to 85°C)
			AT27C080-10PI	32P6	
			AT27C080-10RI	32R	
			AT27C080-10TI	32T	

Package Type	
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
32P6	32-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
32R	32-Lead, 0.450" Wide, Plastic Gull Wing Small Outline (SOIC)
32T	32-Lead, Plastic Thin Small Outline Package (TSOP)



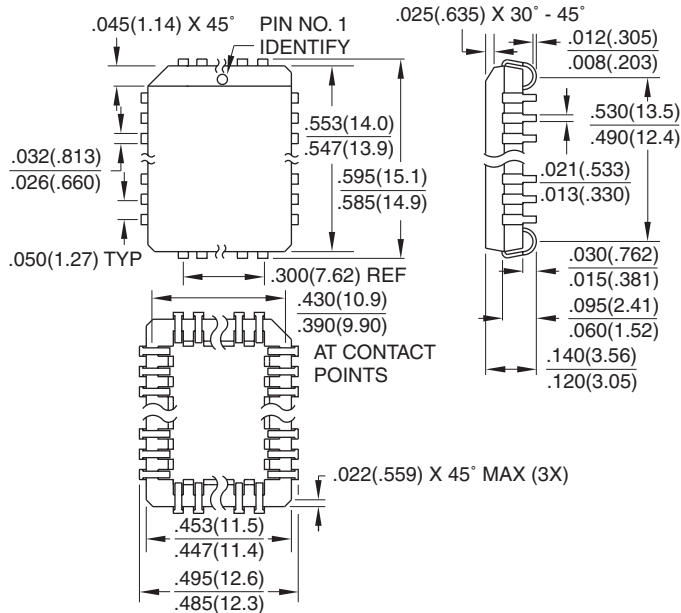
Ordering Information (Continued)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	40	0.1	AT27C080-12JC	32J	Commercial (0°C to 70°C)
			AT27C080-12PC	32P6	
			AT27C080-12RC	32R	
			AT27C080-12TC	32T	
	40	0.1	AT27C080-12JI	32J	Industrial (-40°C to 85°C)
			AT27C080-12PI	32P6	
			AT27C080-12RI	32R	
			AT27C080-12TI	32T	
150	40	0.1	AT27C080-15JC	32J	Commercial (0°C to 70°C)
			AT27C080-15PC	32P6	
			AT27C080-15RC	32R	
			AT27C080-15TC	32T	
	40	0.1	AT27C080-15JI	32J	Industrial (-40°C to 85°C)
			AT27C080-15PI	32P6	
			AT27C080-15RI	32R	
			AT27C080-15TI	32T	

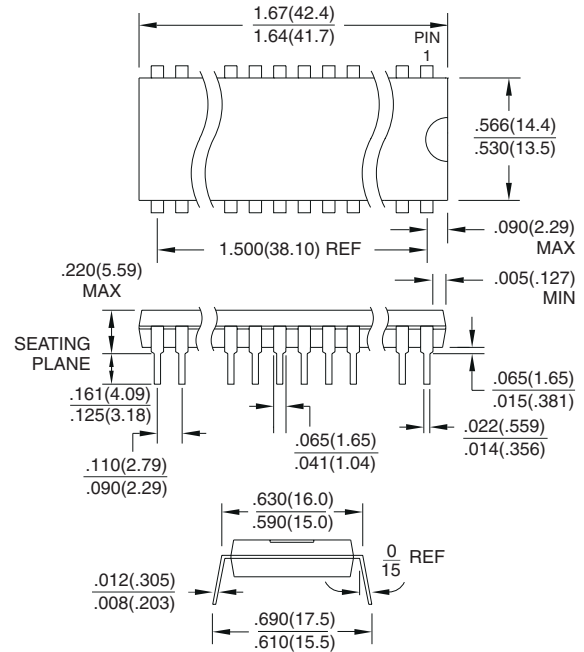
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32R	32-Lead, 0.450" Wide, Plastic Gull Wing Small Outline (SOIC)
32T	32-Lead, Plastic Thin Small Outline Package (TSOP)

Packaging Information

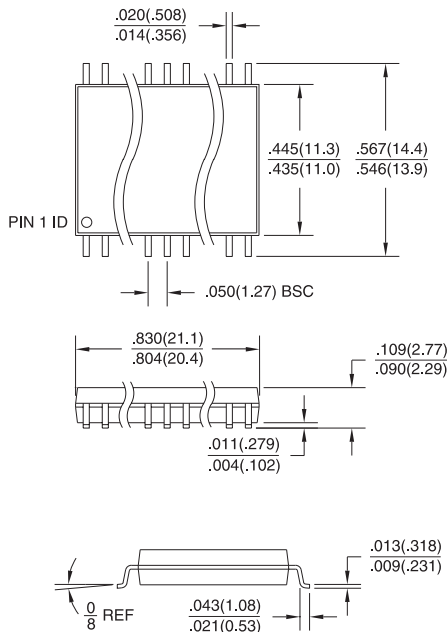
32J, 32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-016 AE



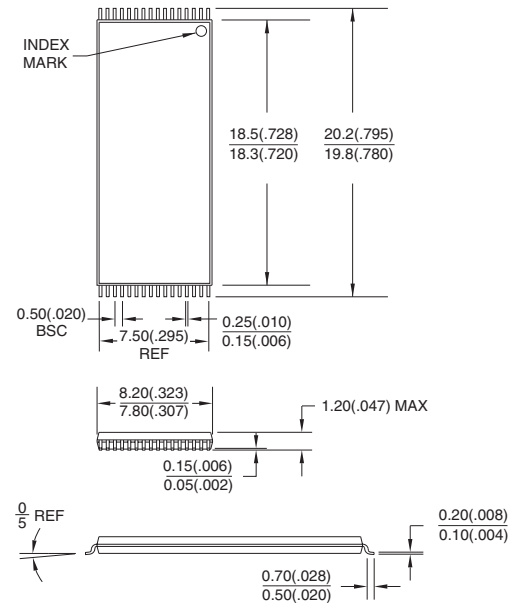
32P6, 32-Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



32R, 32-Lead, 0.440" Wide, Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



32T, 32-Lead, Plastic Thin Small Outline Package (TSOP)
Dimensions in Millimeters and (Inches)*
JEDEC OUTLINE MO-142 BD





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